Claim Amendments

Please amend the claims as follows:

14. (currently amended) A method for the fabrication of a semiconductor assembly comprising:

providing a semiconductor wafer comprising a plurality of undivided integrated circuit chips on a first surface of said wafer, each circuit chip having a plurality of metal contact pads as electrical entry and exit ports;

forming a planar array of solder balls attached to said contact pads of said plurality of chips on said semiconductor wafer so that each of said contact pads is contacted by one of said solder balls;

providing an interposer of electrically insulating material having first and second opposite surfaces and electrically conductive paths from said first surface to said second surface, said conductive paths forming electrical entry and exit ports on said insulating interposer;

applying radiant energy from a first energy source to said interposer and then aligning said interposer with said solder balls so that each port is placed into alignment with one of said solder balls on said semiconductor wafer;

contacting said ports and said solder balls;

applying directed radiant energy from a separately controlled second source to a second surface of said semiconductor wafer such that said wafer increases uniformly in temperature and transfers heat to said solder balls, causing the solder balls to reach a liquid state, said step of applying directed radiant energy from a separately controlled second source performed during said step of applying radiant energy from a first energy source to said interposer;

removing said energy such that said solder balls cool and harden, forming physical bonds between said solder balls and said ports; and

separating the resulting composite structure into discrete chips.

15. (currently amended) A method for the fabrication of a semiconductor assembly comprising:

providing a silicon semiconductor wafer comprising a plurality of undivided integrated circuit chips on a first surface of said wafer, each circuit chip having a plurality of metal contact pads as electrical entry and exit ports;

forming a first planar array of solder balls attached to said contact pads of said plurality of chips on said semiconductor wafer so that each of said contact pads is contacted by one of said solder balls;

providing an interposer of electrically insulating material having first and second opposite surfaces and electrically conductive paths from said first surface to said second surface, said conductive paths forming electrical entry and exit ports on said insulating interposer;

applying radiant energy from a first energy source to said interposer and then aligning said interposer with said solder balls so that each port is placed into alignment with one of said solder balls on said semiconductor wafer;

contacting said ports and said solder balls;

applying directed radiant energy from a separately controlled second source having a wavelength of 0.8 to 2.8 μm to a second surface of said semiconductor wafer such that said wafer increases uniformly in temperature and transfers heat to said solder balls, causing said solder balls to reach a liquid state, said step of applying directed radiant energy from a separately controlled second source performed during said step of applying radiant energy from a first energy source to said interposer;

said wavelength of said second source causing the wafer to heat more rapidly than said interposer;

removing said energy such that said solder balls cool and harden, forming physical bonds between said solder balls and said ports;

forming a second planar array of solder balls attached to said exit ports of said interposer so that each of said exit ports is contacted by one of said solder balls; and

separating the resulting composite structure into discrete chips.

16. (previously amended) A method for the fabrication of a semiconductor assembly comprising:

providing a semiconductor wafer comprising a plurality of undivided integrated circuit chips, each circuit chip having a plurality of metal contact pads as electrical entry and exit ports, said contact pads arranged at a first spacing pitch;

providing an adhesive layer adjacent said wafer, said adhesive layer having first and second opposite surfaces and a multitude of electrically conductive fibers extending through electrically nonconductive material from said first surface to said second surface of the layer while remaining insulated from adjacent fibers, said fibers arranged in said adhesive layer at a second spacing pitch, said second pitch being smaller than said first pitch;

providing an interposer of electrically insulating material having first and second opposite surfaces and electrically conductive paths from said first surface to said second surface, said conductive paths forming electrical entry and exit ports on said insulating interposer;

placing said interposer vertically and in contact with said adhesive substrate;

providing a polymer film having a plurality of discrete adhesive areas;

providing a plurality of solder balls, one of said solder balls being placed on each of said adhesive areas;

aligning said polymer film to said interposer so that each of said solder balls is placed into alignment with one of said ports;

placing said solder balls in contact with said ports;

applying radiant energy to said semiconductor wafer such that said wafer uniformly increases in temperature and transfers heat to said adhesive substrate, said interposer and said solder balls, causing said solder balls to reach a liquid state;

separately controlling the temperature of said interposer in order to minimize differences in thermal expansion;

removing said energy such that all said contacts form physical bonds and said solder balls cool and harden, forming physical bonds between said solder balls and said ports;

removing said polymer film; and

separating the resulting composite structure into discrete chips.

17. (original) The method according to Claim 14, Claim 15, and Claim 16 wherein said solder balls comprise at least one alloy with a melting temperature compatible with multiple reflow.

18. (original) The method according to Claim 14, Claim 15, and Claim 16, wherein said wafer contact pads, said solder balls, and said interposer ports comprise a combination of materials such that metal interdiffusion is minimized.

19. (previously amended) A method as in claim 14, wherein said step of applying radiant energy to said interposer heats said interposer to a temperature in the range of 75 to 80 percent of the temperature that causes said solder balls to reach a liquid state.

20. (previously added) A method as in claim 15, further including the step of preheating said interposer prior to alignment with the wafer.